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Area and Power Optimized D-flip flop and Subtractor

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ABSTRACT

Low power is essential in today's technology. It is most significant with high speed, small size and stability. So, power reduction is most important in modern technology using VLSI design techniques. Today most of the market necessities require low power, long run time and market which also deserve small size and high speed. In this paper several logic circuits DFF with 5 transistors and sub tractor circuit using powerless XOR gate and Groundless XNOR gates are implemented. In the proposed DFF, the area can be decreased by 62% & substarctor circuit, area decreased by 80% and power consumption of DFF and subtractor circuit are 15.4µW and 13.76µW respectively, but these are very less as compared to existing techniques.

Keywords: *D FF, NMOS, PMOS, VLSI, P-XOR, G-XNOR*

i. INTRODUCTION

In a large or small circuits, power dissipation is a significant constraint in design process. Today Low power designs are very essential because of most of the embedded and IoT systems are operated with the batteries. The Embedded system consuming more power then battery to be charged more number of times in turns battery life will be decreased. It indicates maintenance cost of the device increases. So most of the devises particularly medical implanted devices need to be consumed low power. So low power is a new era in VLSI technology, as it influences many IoT or Embedded System applications. But today designers not only concentrating on consumption of power, also concentrating speed of the circuit. Now there is huge demand from the customers and designers to be concentrating on the power dissipation in digital circuits. In digital circuits, logic gates may be interconnection of logic gates to perform the desired functionality with one or more input signals. Due to the signal changes, producing signal transition, this current cause's capacitive load of CMOS gate can be charged or discharged which will effects the power dissipation of the digital circuit.

ii. LITERATURE SURVEY

In the era of microelectronics, power dissipation is limiting factor. In any CMOS technology, provides very low Static power dissipation. Due to the discharge of capacitance, during the switching operation, that cause a power dissipation. Which increases with the clock frequency. Using Transmission Gate Technique Such unnecessary discharging can be prevented. Due to the resistance of switches, impartial losses may be occurred for any logic operation.

To avoid these minor losses keep clock frequency to be small than the technological limit. There are different types of Transmission Gate logic families. But each family shows some merits and some limitations for logical circuits. But Transmission Gate families can be categorized as either partially/quasi Adiabatic or fully Transmission Gate. Some charge is permitted to be transferred to the ground in a partially/quasi Transmission Gate circuit. The power supply recovers the all the charge on the load capacitance in a fully Transmission Gate circuit. Fully Transmission Gate circuits are facing problems like operating speed and the

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input power clock synchronization.

iii. D- FF (FLIP FLOP) CIRCUIT

In an IC design, Power consumption is very vital role. Flip flops are categorized as single and double edge triggered. In a Single edge triggered FF, data sampling can be on rising or on falling edge of clock. In an double edge triggered, dat can be sampled on both the clock edges. But this FF delivers poor performance and difficult to design also. The other types of FFs are static and dynamic flip-flops. The dynamic FF having a drawback of producing faulty logic levels, whenever the clock is detached, due to the charge leakage from the output node capacitances. But in static FF, it keeps state as it is even though there is no clock.

In most of the conventional FF implementations, more transistors to be active and occupies large area. The designers are introduced numerous effective designs. But Still designers are looking for new designs which occupies less area and their power consumption to be low. In this paper proposed new DFF , implemented with few transistors and occupies less area and consumes less power.

In most common flip flops are JK flip flop, T flip flop, D flip flop out of these D flip flop is simple. Another name for Dff is delay or data flip flop. This flip flop stores the bit/bits when the clock is arrived. The output of the Dff will be at Q, and does not change until input changes and clock arrival occurs.

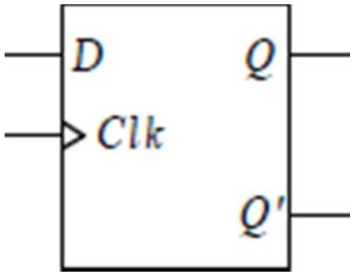

Figure 1: D FF Symbol

Table 1: D flip flop Excitation table

Q	Q^1	Q_{NEXT}	D
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1

Particularly to store the bit information, latches and flip flops are the simple basic elements.

The major difference between latches and flip flops are latches changes its state only on the enabled signal, but in flip flops its states changes only on the edge of the clock signal. But contents remains constant in the flip flop even though changers in the inputs.

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iv. New D FLIP FLOP DESIGN

The new D FF (Flip flop) circuit shown in Figure 2. It consists of a basic two-inverter loop and two CMOS transmission gate (TG) switches. The clock signal which triggers the TG, the reverse of the clock signal triggers the TG which is in the inverter loop. So when the clock is high, the input signal is accepted (latched) into the circuit, and this data is conserved as the state of the inverter loop when clock is low.

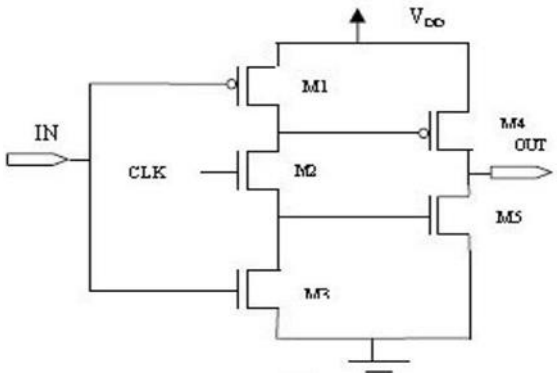

Figure 2: New D Flip flop using 5 transistors

The clock signal and input IN tied to high, then M1, M5 transistors shows OFF condition and M2, M3, M4 transistors shows ON. The output becomes high. For the entire clock period, the value of input, it becomes output.
In any high performance VLSI systems, there is a need of Minimum power consumption. In any digital CMOS circuit, three types of power dissipation, there are 1. it is due to signal transition 2. it is due to short circuit current 3. due to leakage currents.

v. SUBTRACTOR CIRCUIT

INTRODUCTION

Most of the simple logic circuits of arithmetic are modeled by XOR-XNOR gates. Full adders / sub tractor are the basic buildings of arithmetic logic units. The design of low power consumed Full sub tractor circuit is very essential in many of the circuits. The XOR/XNOR circuits are the major contributors of power dissipation in full subs tractor circuits. In this approach while implementation of full substractor circuit, uses one XOR or XNOR gate to implement a full subtractor..

vi. LOW POWER SUBTRACTOR CIRCUIT

Normally conventional full subtractor circuit having more delay , area and more power dissipation as the conventional gates consists of more number of transistors.

The algebraic expressions for XOR are as follows:

$$A \cdot \overline{B} + \overline{A} \cdot B$$

The conventional implementation of XOR gate for CMOS shown in Figure 3 and conventional

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XNOR gate shown in Figure 4. Truth tables of XOR gate and XNOR gate shown in Table 2 and 3.

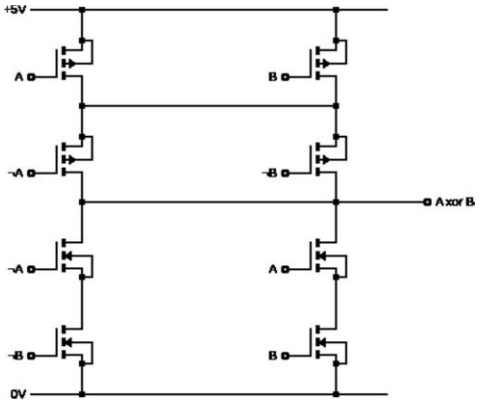
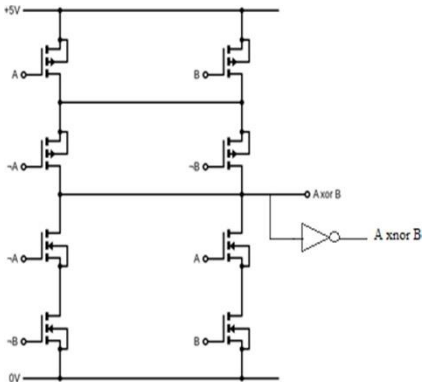


Figure 3: Conventional XOR Gate

Table 2: Truth Table for XOR Gate



INPUTS		OUTPUTS
A	B	Y = A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

Table 3: Truth Table for XNOR Gate

Inputs		Outputs
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	1

The powerless P-XOR gate shown in Figure 5 consumes less power because of power is not connected. The ground less G-XNOR shown in Figure 6, which also consuming lesser power. Particularly for low power applications, use the Pass-Transistor Logic. This technique is a efficient technique to reduce the power of the logic circuits. In any PTL network, either NMOS or PMOS is enough to get the desired logic operation, which leads to lesser number

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transistors and considerable input loads when NMOS network is used. The short – circuit energy dissipation may be occurred due to VDD-to- GND paths, this leads to short-circuit energy dissipation.

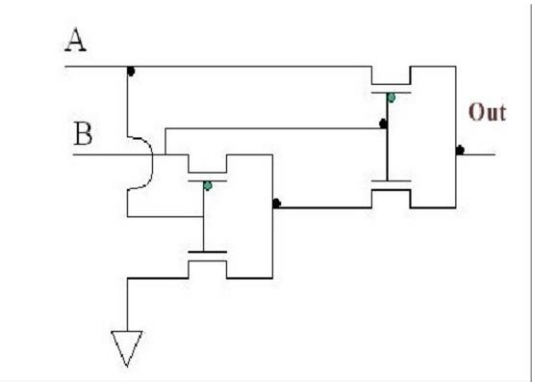


Figure 5: Powerless XOR(P-XOR) Gate

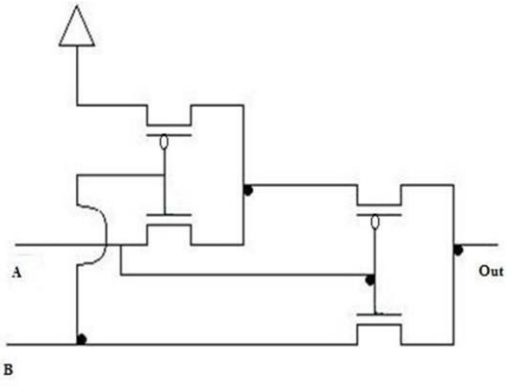
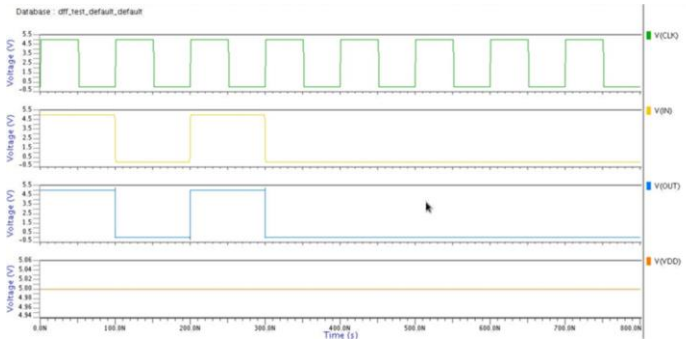


Figure 6: Groundless XNOR **(**G-XNOR) Gate

vii. RESULTS

The designs are implemented using Mentor graphics tool and verified with simulator tools. The results are shown in Figure 7-11. The output of the DFF shown in Figure 7,the delayed DFF output shown in Figure 8, Power out put of DFF shown in Figure 9. The schematic diagram of DFF shown in Figure 10 and schematic diagram of subtractor circuit shown in Figure 11.

Figure 7: Output of D Flip flop



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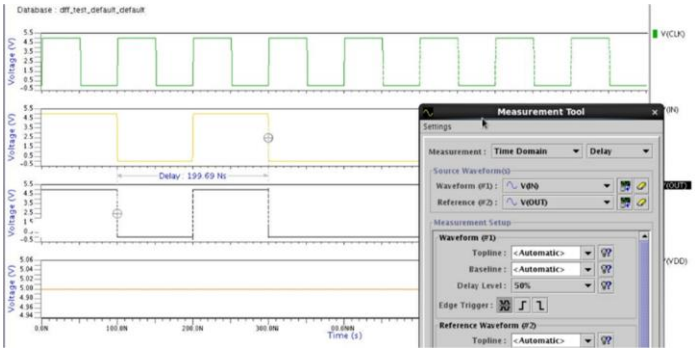

Figure 8: Delayed Output of D Flip flop

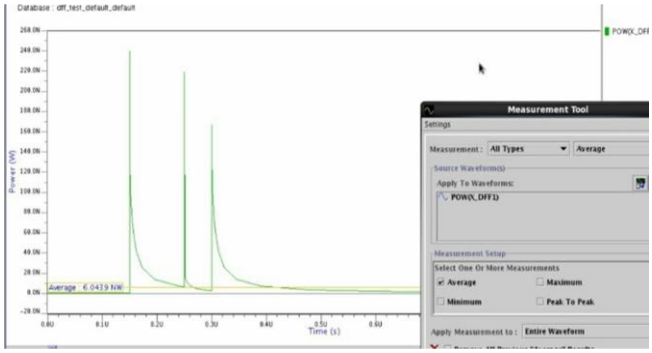

Figure 9: Power Output of D Flip flop

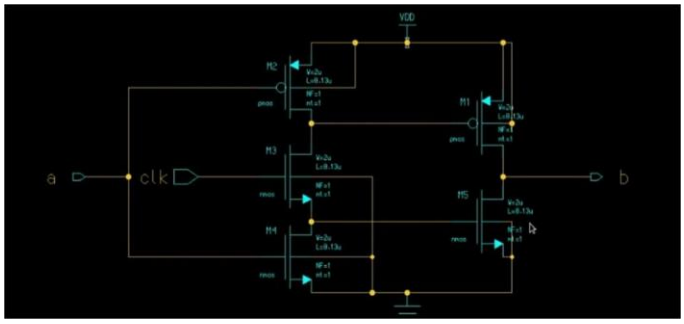

Figure 10: Schematic of D Flip flop

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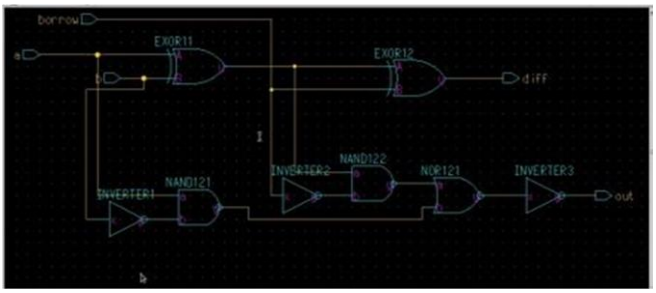

Figure 11: Schematic of Subtractor

i. POWER DISSIPATION

In any logic circuit, there will be two parameters playing key role in the design of required circuits, are power dissipation and area. When the count of transistors are increasing, normally power dissipation may be enlarged along with area also enlarged, this is drawback of the circuits. But still moores law is existing, every 18months , number of transistors may be doubles, which was possible only reducing the scaling the various parameters of transistors.

Table 4: Power Dissipation of D Flip flop.

Name of the Circuit	Parameter	Proposed Circuit	Existing Circuit
D Flip flop	Power Dissipation	15.4µW	20.073µW

Table 5: Power Dissipation of Subtractor Circuit.

Name of the Circuit	Parameter	Proposed Circuit	Existing Circuit
Subtractor	Power Dissipation	13.76µW	56µW

ii. AREA

For making an area efficient circuit, there is need of efficient algorithm for digital circuits. With the help of Clock period management, the sequential circuits can be operated in a efficient manner. The size of the gate also influence on the area occupied by the circuits. In this work, always trying to reduce the number of transistors also to reduce the area which are occupied by the transistors. The results of D-FF and Subtractor circuit are tabulated in Table 6 & Table 7.

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Table 6: Area Results for D Flip Flop Circuit

Name of the Circuit	Parameter	Proposed Circuit	Existing Circuit
D Flip-flop	Area(in no.of transistors)	05	08

Table 7: Area Results for Sub tractor Circuit

Name of the Circuit	Parameter	Proposed Circuit	Existing Circuit
sub tractor	Area(in no.of Transistors)	23	28

CONCLUSION

FFs and subtractor circuits are the circuits which are comprehensively used in ALU operations. As they are regularly used in the systems they would dissipate less power related to the other circuits. So a special type of logic has been introduced called Transmission Logic which depresses the power dissipation of this kind of circuits. Circuits intended with Transmission Logic style have comparatively less Power Dissipation to that of CMOS Logic style. In the designed DFF and Subtractor circuits are occupied less are and consumes less power as compared to existing techniques. Particularly in an subtractor circuit power consumption is 13.76µW.

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